Claims

Sub A1

1. An improved CMOS integrated imager system having an array of pixel areas with at least one control area, wherein said pixel areas include a plurality of light collecting elements which each receive light and store electronic information in an amount indicative of an amount of light received during an integration period, with the control area having an internal timing element, wherein the improvement comprises:

an interface for receiving a plurality of data, address, and control signals, said interface receiving a mode signal for setting the system in one of a first operating mode or a second operating mode characterized in that the first operating mode uses the internal timing element to control timing operation of the system and the second operating mode bypasses the internal timing element to control timing operation of the system.

2. The imager system of Claim 1, wherein the control area includes a data bus, an address bus and a control bus electrically coupled to the interface and further includes a bypass multiplexer connected to the control bus, said multiplexer operating to interconnect the internal timing element to the control bus upon receipt of a first mode signal and operating to bypass the internal control element upon receipt of a second mode signal.

3. The imager system of Claim 1, further including means for receiving timing signals from an external timing element when the system is operating in the second operating mode.

4. The imager system of Claim 3, wherein the external timing element includes an external timing generator and a color recovery block.

Sub A2

5. The imager system of Claim 3, wherein the external timing block includes a memory and a DMA interface block.

6. The imager system of Claim 1, wherein the imager operates in the first operating mode when the interface is not connected to receive the mode signal.

7. A timing selector for a CMOS integrated imager comprising:

an onboard timing means, associated with a CMOS integrated imager, for providing standard timing signals to operate a clock circuit aboard the integrated imager;

an outboard logic circuit electrically connected to the CMOS integrated imager generating signals established by a user for establishing user defined timing signals for customized imager operation, and

a user interface allowing selection of the onboard timing means or outboard logic circuit.

8. The apparatus of Claim 7, wherein the outboard logic circuit has means for generating clock signals bypassing the clock circuit.

9. The apparatus of Claim 7, wherein the outboard logic circuit has means for generating clock signals using the clock circuit.